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10/551,415	11/17/2005	Toshiyuki Oga	Q90624	4446

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/551,415	OGA, TOSHIYUKI	
	Examiner	Art Unit	
	Tuan H. Nguyen	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 09/30/2005 and 11/17/2005 has been considered by Examiner and made of record in the application file.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The

abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 16, 20, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Imura Shigeru et al. (Japanese Publication Number: 08-149035 hereinafter, "Imura").

Consider claim 16, Imura teaches information processing terminal system comprising: an information processing terminal (page 3 [0029]); and a transmitting and receiving unit which can be attached to and detached from said information processing

terminal (page 3 [0030]), wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, a modulation section and a baseband processing section (page 2 [0018]-[0020] and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 3 [0020]), said baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal said modulation section converts the transmission analog baseband signal into a transmission modulation wave signal (page 3 [0020]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into a reception data and converts a transmission data into the transmission digital baseband signal (page 3 [0020] and [0021]).

Consider claim 20, Imura teaches a transmitting and receiving method in an information processing terminal system in which a detachable transmitting and receiving unit is attached to an information processing terminal, comprising:

(h) in said transmitting and receiving unit, demodulating a reception modulation wave

signal from a network to convert into a reception analog baseband signal (page 3 [0021]); (i) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital baseband signal (page 2 [0020]); (j) in said information processing terminal, converting the reception digital baseband signal into a reception data (page 2 [0020]); (k) in said information processing terminal, converting a transmission data into a transmission digital baseband signal (page 2 [0020]); (l) in said transmitting and receiving unit, converting the transmission digital baseband signal into a transmission analog baseband signal (page 2 [0020]); (m) in said transmitting and receiving unit, converting the transmission analog baseband signal into a transmission modulation wave signal (page 2 [0020]); and (n) in said transmitting and receiving unit, transmitting the transmission modulation wave signal to the network (page 3 [0026]).

Consider claim 27, Imura teaches a transmitting and receiving unit in an information processing terminal system comprising an information processing terminal and said transmitting and receiving unit which can be attached to or detached from said information processing terminal, wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, an modulation section and a baseband processing section (page 2 [0020] and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said

network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]), said baseband processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal from said information processing terminal into a transmission analog baseband signal (page 2 [0020] and page 3 [0021]), and said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal (page 2 [0020]).

Consider claim 28, Imura teaches an information processing terminal in an information processing terminal system comprising said information processing terminal and a transmitting and receiving unit which can be attached to or detached from said information processing terminal (page 2 [0020] and page 3 [0021]), wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, an modulation section and a baseband processing section (page 2 [0018]-[0020] and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to said network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]), said baseband

processing section converts the reception analog baseband signal into a reception digital baseband signal and converts a transmission digital baseband signal from said information processing terminal into a transmission analog baseband signal (page 2 [0020]), said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal (page 2 [0020]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts a transmission data into the transmission digital baseband signal (page 2 [0020] and page 3 [0021]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 9, 17-19, and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura Shigeru et al. (Japanese Publication Number: 08-149035 hereinafter, "Imura") in view of Miller (U.S PAT. 6,700,943).

Consider claims 1 and 21, Imura teaches an information processing terminal system comprising: an information processing terminal (page 3 [0029]); and a transmitting and receiving unit which can be attached to or detached from said

information processing terminal (page 3 [0030]), wherein said transmitting and receiving unit comprises: a transmission and reception processing section; a demodulation section; a modulation section and a baseband processing section (page 2 [0018]-[0020]) and page 3 [0021]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission modulation wave signal from said modulation section to the network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]), said baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal, and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal (page 2 [0020]) and page 3 [0021]), said modulation section converts the transmission analog baseband signal into the transmission modulation wave signal (page 2 [0020]).

Imura does not explicitly show that baseband processing section and information processing terminal operate in synchronization with a clock, and the reception digital signal contains a reception data, and the transmission digital signal contains a transmission data.

In the same field of endeavor, Miller teaches baseband processing section and information processing terminal operate in synchronization with a clock (col. 2 lines 35-

46), and the reception digital signal contains a reception data, and the transmission digital signal contains a transmission data (col. 2 lines 35-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, baseband processing section and information processing terminal operate in synchronization with a clock, and the reception digital signal contains a reception data, and the transmission digital signal contains a transmission data, as taught by Miller, in order to provide an apparatus and method for synchronizing a derived bit clock with a transmit bit clock of a transmitted data signal.

Consider claim 2, Imura further teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal as the reception digital signal to output to said information processing terminal (page 3 [0021]); and converts a transmission digital baseband signal as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts the transmission data into the transmission digital baseband signal (page 2 [0020]).

Consider claim 9, Imura further teaches said baseband processing section converts the reception analog baseband signal into the reception data as the reception digital signal to output to said information processing terminal and converts the

transmission data as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020]) and page 3 [0021]).

Consider claim 17, Imura teaches a transmitting and receiving method in an information processing terminal system in which a detachable transmitting and receiving unit is attached to an information processing terminal, comprising:
(a) in said transmitting and receiving unit, demodulating a reception modulation wave signal from a network to convert into a reception analog baseband signal (page 2 [0020]) and page 3 [0021]); (f) in said transmitting and receiving unit, converting the transmission analog baseband signal into a transmission modulation wave signal (page 2 [0020]); and (g) in said transmitting and receiving unit, transmitting the converted transmission modulation wave signal to the network (page 3 [0026]).

Imura does not explicitly show that (b) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital signal containing a reception data in synchronization with a clock; (c) in said information processing terminal, receiving the reception digital signal in synchronization with a clock; (d) in said information processing terminal, sending a transmission digital signal containing a transmission data in synchronization with the clock; (e) in said transmitting and receiving unit, converting the transmission digital signal into a transmission analog baseband signal in synchronization with the clock.

In the same field of endeavor, Miller teaches (b) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital signal containing a reception data in synchronization with a clock (col. 2 lines 35-46); (c) in said information processing terminal, receiving the reception digital signal in synchronization with a clock (col. 2 lines 35-46); (d) in said information processing terminal, sending a transmission digital signal containing a transmission data in synchronization with the clock (col. 2 lines 35-46); (e) in said transmitting and receiving unit, converting the transmission digital signal into a transmission analog baseband signal in synchronization with the clock (col. 2 lines 35-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, (b) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital signal containing a reception data in synchronization with a clock; (c) in said information processing terminal, receiving the reception digital signal in synchronization with a clock; (d) in said information processing terminal, sending a transmission digital signal containing a transmission data in synchronization with the clock; (e) in said transmitting and receiving unit, converting the transmission digital signal into a transmission analog baseband signal in synchronization with the clock, as taught by Miller, in order to provide an apparatus and method for synchronizing a derived bit clock with a transmit bit clock of a transmitted data signal.

Consider claim 18, Imura further teaches wherein said (b) comprises (b1) in said transmitting and receiving unit, converting the reception analog baseband signal into a reception digital baseband signal as the reception digital signal (page 2 [0020]), said (c) comprises (c1) in said information processing terminal, converting the reception digital baseband signal into the reception data (page 3 [0021]), said (d) comprises (d1) in said information processing terminal, converting the transmission data into a transmission digital baseband signal as the transmission digital signal (page 2 [0020]), and said (e) comprises (e1) in said transmitting and receiving unit, converting the transmission digital baseband signal into the transmission analog baseband signal (page 2 [0020]).

Consider claim 19, Imura further teaches wherein said (b) comprises (b2) in said transmitting and receiving unit, converting the reception analog baseband signal into the reception data as the reception digital signal, said (c) comprises (c2) in said information processing terminal, receiving the reception data (page 2 [0020]), said (d) comprises (d2) in said information processing terminal, outputting the transmission data as the transmission digital signal to said transmitting and receiving unit (page 3 [0021]), and said (e) comprises (e2) in said transmitting and receiving unit, converting the transmission data into the transmission analog baseband signal (page 2 [0020]).

Consider claim 22, Imura further teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal as the reception digital signal to output to said information processing terminal, and converts a

transmission digital baseband signal as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020] and page 3 [0021]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts the transmission data into the transmission digital baseband signal (page 2 [0020]).

Consider claim 23, Imura further teaches baseband processing section converts the reception analog baseband signal into the reception data as the reception digital signal to output to said information processing terminal, and the transmission data as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020] and page 3 [0021]).

Consider claim 24, Imura teaches an information processing terminal in an information processing terminal system comprising said information processing terminal and a transmitting and receiving unit which can be attached to or detached from said information processing terminal (page 3 [0030]), wherein said transmitting and receiving unit comprises a transmission and reception processing section, a demodulation section, a modulation section and a baseband processing section (page 2 [0020]), when said transmitting and receiving unit is attached to said information processing terminal, said transmission and reception processing section outputs a reception modulation wave signal from a network to said demodulation section and transmits a transmission

modulation wave signal from said modulation section to said network (page 3 [0026]), said demodulation section converts the reception modulation wave signal from said transmission and reception processing section into a reception analog baseband signal (page 2 [0020]), said baseband processing section converts the reception analog baseband signal into a reception digital signal to output to said information processing terminal and converts a transmission digital signal from said information processing terminal into a transmission analog baseband signal (page 2 [0020] and page 3 [0021]), said modulation section converts the transmission analog baseband signal into a transmission modulation wave signal (page 2 [0020]), and the reception digital signal contains a reception data and the transmission digital signal contains a transmission data (page 2 [0020]).

Imura does not explicitly show that baseband processing section and said information processing terminal operate in synchronization with the clock.

In the same field of endeavor, Miller teaches baseband processing section and said information processing terminal operate in synchronization with the clock (col. 2 lines 35-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, baseband processing section and said information processing terminal operate in synchronization with the clock, as taught by Miller, in order to provide an apparatus and method for synchronizing a derived bit clock with a transmit bit clock of a transmitted data signal.

Consider claim 25, Imura further teaches baseband processing section converts the reception analog baseband signal into a reception digital baseband signal as the reception digital signal to output to said information processing terminal, and converts a transmission digital baseband signal as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 2 [0020] and page 3 [0021]), and said information processing terminal converts the reception digital baseband signal from said baseband processing section into the reception data and converts the transmission data into the transmission digital baseband signal (page 2 [0020]).

Consider claim 26, Imura further teaches baseband processing section converts the reception analog baseband signal into the reception data as the reception digital signal to output to said information processing terminal (page 2 [0020]), and converts the transmission data as the transmission digital signal from said information processing terminal into the transmission analog baseband signal (page 3 [0021]).

8. Claims 3-8 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura in view of Miller, and further in view of Philips et al. (U.S PUB. 2003/0118081 hereinafter, "Philips").

Consider claim 3, Imura and Miller, in combination, fails to teaches information processing terminal comprises: an interface; and a control unit configured to convert the

reception digital baseband signal supplied through said interface from said baseband processing section into the reception data and the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface, and said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said control unit as a clock.

However, Philips teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data and the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), and said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said control unit as a clock (page 4 [0046]).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Philips into view of Imura and Miller, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Consider claim 4, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband

processing section into the reception data, and to convert the transmission data into said transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), said demodulation section generates and outputs a reception symbol clock having a frequency to said clock generator (page 3 [0035]), said clock generator generates a second reception symbol clock based on the reception symbol clock from said demodulation section to output to said baseband processing section, said interface and said control unit as a clock (page 3 [0038]), and the second reception symbol clock is synchronous with the reception symbol clock and has a frequency different from a frequency of the reception symbol clock (page 15 [0265]).

Consider claim 5, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data; and to convert the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]); and a clock generator (page 3 [0035]), said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said clock generator as a clock (page 3 [0035]), said clock generator receives the reception symbol clock from the demodulation section as a first clock, generates and outputs a second clock

synchronous with the first clock to said control unit as a clock, and generates the second clock through self-oscillation to output to said control unit as a clock, when the first clock is not supplied (page 5 [0077]).

Consider claim 6, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data; and to convert the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 4 [0045]), said transmission and reception processing section generates and outputs a reference signal having a frequency to said clock generator (page 4 [0045]), said clock generator recovers a carrier of the reception modulation wave signal based on the reference signal from said transmission and reception processing section to output to said demodulation section; and generates and outputs a reception symbol clock to said baseband processing section, said interface and said control unit as a clock (page 3 [0038]), said reception symbol clock is synchronous with the reference signal (page 3 [0035]), and said demodulation section, said baseband processing section, said interface and said control unit operate in synchronization with the reception symbol clock (page 3 [0035]).

Consider claims 7 and 14, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data (page 4 [0046]); and to convert the transmission data into the transmission digital baseband signal to output to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claim 8, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); a control unit configured to convert the reception digital baseband signal supplied through said interface from said baseband processing section into the reception data (page 4 [0045]); and a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claim 10, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section and to output the transmission data to said baseband processing section through said interface

(page 4 [0046]), and said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband processing section, said interface and said control unit as a clock (page 3 [0035]).

Consider claim 11, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit baseband processing section and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), said demodulation section generates and outputs a reception symbol clock having a frequency to said clock generator (page 3 [0035]), said clock generator generates a second reception symbol clock based on the reception symbol clock from said demodulation section to output to said baseband processing section, said interface and said control unit as a clock (page 3 [0035]), and said second reception symbol clock is synchronous with the reception symbol clock and has a frequency different from the frequency of the reception symbol clock (page 3 [0035]).

Consider claim 12, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); a control unit configured to receive the reception data through said interface from said baseband processing section and to output the transmission data to said baseband processing section through said interface (page 4 [0046]); and a clock generator (page 3 [0035]), said demodulation section generates and outputs a reception symbol clock having a frequency to said baseband

processing section, said interface and said clock generator as the clock (page 3 [0035]), and said clock generator receives the reception symbol clock from said demodulation section as a first clock, generates and outputs a second clock synchronous with the first clock to said control unit as a clock, and generates the second clock through self-oscillation to output to said control unit as the clock when the first clock is not received (page 5 [0077]).

Consider claim 13, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section, and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), said transmission and reception processing section generates and outputs a reference signal having a frequency to said clock generator (page 4 [0045]), said clock generator recovers a carrier of the reception modulation wave signal based on the reference signal from said transmission and reception processing section to output to the demodulation section, and generates and outputs a reception symbol clock to said baseband processing section, said interface and said control unit as a clock (page 3 [0038]), said reception symbol clock is synchronous with the reference signal, and said demodulation section, said baseband processing section, said interface and the control unit operate in synchronization with the reception symbol clock (page 3 [0035]).

Consider claim 14, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section, and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

Consider claim 15, Philips further teaches information processing terminal comprises: an interface (page 4 [0045]); and a control unit configured to receive the reception data through said interface from said baseband processing section, and to output the transmission data to said baseband processing section through said interface (page 4 [0046]), said transmitting and receiving unit further comprises a clock generator (page 3 [0035]), and said clock generator generates a clock through self-oscillation to output to said baseband processing section, said interface and said control unit (page 3 [0038]).

9. Claims 29-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura in view of Philips.

Consider claim 29, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit, wherein said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal (see fig. 10 page 2 [0016]).

Imura does not explicitly show that a clock generating circuit configured to generate a clock; and a first interface configured to operate in response to said clock, and said signal processing unit comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces.

In the same field of endeavor, Philips teaches a clock generating circuit configured to generate a clock (page 3 [0035]); and a first interface configured to operate in response to said clock (page 3 [0035]), and said signal processing unit comprises: a second interface connected with said first interface and configured to operate in response to said clock (page 4 [0046] and page 5 [0062]; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces (page 8 [0130]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, a clock generating circuit configured to generate a clock; and a first interface configured to operate in response to said clock, and said signal processing unit comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section

configured to demodulate said reception digital signal supplied through said first and second interfaces, as taught by Philips, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Consider claim 39, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit (page 1 [0016]).

Imura does not explicitly show that signal processing unit comprises: a clock generating circuit configured to generate a clock; said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal; and a first interface configured to operate in response to said clock, and said signal processing unit further comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces.

In the same field of endeavor, Philips teaches signal processing unit comprises: a clock generating circuit configured to generate a clock (page 3 [0035]); said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal; and a first interface configured to operate in response to said clock (page 3 [0035]), and said signal processing unit further comprises: a second interface connected with said first interface and configured to

operate in response to said clock (page 4 [0046] and page 5 [0062]); and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces (page 8 [0130]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, signal processing unit comprises: a clock generating circuit configured to generate a clock; said radio unit comprises: a reception signal converting circuit configured to generate a reception digital signal from a reception radio signal; and a first interface configured to operate in response to said clock, and said signal processing unit further comprises: a second interface connected with said first interface and configured to operate in response to said clock; and a demodulation section configured to demodulate said reception digital signal supplied through said first and second interfaces, as taught by Philips, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Consider claims 30 and 40, Philips further teaches reception signal converting circuit operates in response to said clock (page 3 [0035]).

Consider claims 31 and 41, Philips further teaches demodulation section operates in response to said clock (page 3 [0038]).

Consider claims 32 and 42, Philips further teaches signal processing unit further comprises: a supply circuit configured to supply a transmission digital signal to said radio unit through said second interface (page 3 [0035]), and said radio unit further comprises: a transmission signal converting circuit configured to generate said a transmission radio signal from said transmission digital signal supplied through said first and second interfaces (page 8 [0130]).

Consider claims 33 and 43, Philips further teaches supply circuit operates in response to said clock (page 3 [0035]).

Consider claims 34 and 44, Philips further teaches transmission signal converting circuit operates in response to said clock (page 3 [0035]).

Consider claims 35 and 45, Philips further teaches signal processing unit further comprises: a supply circuit configured to supply a transmission digital signal to said radio unit through said second interface (page 3 [0035]), and said radio unit further comprises: a transmission signal converting circuit configured to generate said a transmission radio signal from said transmission digital signal supplied through said first and second interfaces (page 8 [0130]).

Consider claims 36 and 46, Philips further teaches supply circuit operates in response to said clock (page 3 [0038]).

Consider claims 37 and 47, Philips further teaches transmission signal converting circuit operates in response to said clock (page 3 [0035]).

Consider claims 38 and 48, Philips further teaches one of said first and second interfaces has a parallel bit converting function (page 9 [0142]).

Consider claim 49, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit (see fig. 10 page 2 [0016]).

Imura does not explicitly show that radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; clock generating means for generating a clock; and first interface means for operating in response to said clock, and said signal processing unit comprises: second interface means connected with said first interface means for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interface means

In the same field of endeavor, Philips teaches radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal (page 10 [0157]); clock generating means for generating a clock (page 3 [0035]); and first interface means for operating in response to said clock (page 3 [0035]), and said signal processing unit comprises: second interface means connected with said first

interface means for operating in response to said clock (page 4 [0046] and page 5 [0062]); and demodulation means for demodulating said reception digital signal supplied through said first and second interface means (page 8 [0130]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; clock generating means for generating a clock; and first interface means for operating in response to said clock, and said signal processing unit comprises: second interface means connected with said first interface means for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interface means, as taught by Philips, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Consider claim 50, Imura teaches a radio system comprising: a radio unit (page 3 [0030]); and a signal processing unit provided separately from said radio unit, (see fig. 10 page 2 [0016]).

Imura does not explicitly show that signal processing unit comprises: clock generating means for generating a clock, said radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; and first interface means for operating in response to said clock, and said signal processing unit further comprises: a second interface means connected with said first

interface, for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interfaces.

In the same field of endeavor, Philips teaches signal processing unit comprises: clock generating means for generating a clock, said radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal (page 3 [0035]); and first interface means for operating in response to said clock (page 3 [0035]), and said signal processing unit further comprises: a second interface means connected with said first interface, for operating in response to said clock (page 4 [0046] and page 5 [0062]); and demodulation means for demodulating said reception digital signal supplied through said first and second interfaces (page 8 [0130]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, signal processing unit comprises: clock generating means for generating a clock, said radio unit comprises: reception signal converting means for generating a reception digital signal from a reception radio signal; and first interface means for operating in response to said clock, and said signal processing unit further comprises: a second interface means connected with said first interface, for operating in response to said clock; and demodulation means for demodulating said reception digital signal supplied through said first and second interfaces, as taught by Philips, in order to provide cost-effective and robust modems for use in a wide application area, a high level of programmability and a high degree of integration is preferred.

Conclusion

10. Any response to this action should be mailed to:

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571) 272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Tuan Nguyen T.N
Examiner
Art Unit 2618

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SUPERVISORY PATENT EXAMINER